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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,241	10/08/2003	Chao-Cheng Lee	3722-0164P	5832
2292	7590	06/17/2004	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				COX, CASSANDRA F
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/680,241	LEE ET AL.
Examiner	Art Unit	
Cassandra Cox	2816	<i>Avd</i>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 08 October 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 1-9 is/are allowed.

6) Claim(s) 10-12, 14, 15, 17 and 18 is/are rejected.

7) Claim(s) 13, 16, 19 and 20 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 08 October 2003 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 04/26/04.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

Oath/Declaration

It does not identify the citizenship of each inventor.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 10-12, 14-15, and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi et al. (U.S. Patent No. 6,545,926).

In reference to claim 10, Ooishi discloses in Figure 24 a circuit apparatus operable under a specified operation voltage, the circuit apparatus comprising: a first transistor (N12, N13, N11) having a first breakdown voltage and operating under a first operation voltage; and an interface unit (N16) coupled to the first transistor (N11-N13) for preventing the first operation voltage higher than the first breakdown voltage (see specification column 2, lines 19-23).

In reference to claim 12, the first transistor (N11-N13) is an NMOS transistor. The same applies to claim 11 wherein it is considered well known in the art that NMOS and PMOS transistors can be used interchangeably by reversing their orientation, of which fact official notice is taken.

In reference to claim 14, Ooishi discloses in Figure 24 that the interface unit is a second transistor (N16).

In reference to claim 15, the second transistor (N16) is seen to have a second breakdown voltage that is higher than the first breakdown voltage.

In reference to claim 17, the second transistor (N16) is an NMOS transistor. The same applies to claim 18 wherein it is considered well known in the art that NMOS and PMOS transistors can be used interchangeably by reversing their orientation, of which fact official notice is taken.

Allowable Subject Matter

3. Claims 1-9 are allowed.
4. Claims 13, 16, and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
5. The following is a statement of reasons for the indication of allowable subject matter: Claim 13 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the interface unit comprises: a capacitor (34) coupled to the resistor (32) in parallel in combination with the rest of the limitations of the base claims and any intervening claims. Claim 16 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the second transistor (30) has a gate for receiving a first control signal (V_{PS1}) to make the apparatus in a power-saving mode in combination with the rest of the limitations of the

base claims and any intervening claims. Claim 19 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein the second transistor (30) is a CMOS transistor (36, 38) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 20 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the second transistor (30) operates in a triode region or a saturation region (see specification page 6, lines 8-9) in combination with the rest of the limitations of the base claims and any intervening claims.

6. The following is an examiner's statement of reasons for allowance: Claims 1-9 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 1 wherein the apparatus includes an interface unit (30) serially coupled to a first transistor (10), having a first breakdown voltage and operating under a first operation voltage, and a second transistor (20), having a second breakdown voltage and operating under a second operation voltage, for preventing the first operation voltage higher than the first breakdown voltage and the second operation voltage higher than the second breakdown voltage; wherein the specified operation voltage is higher than both the first operation voltage and the second operation voltage in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

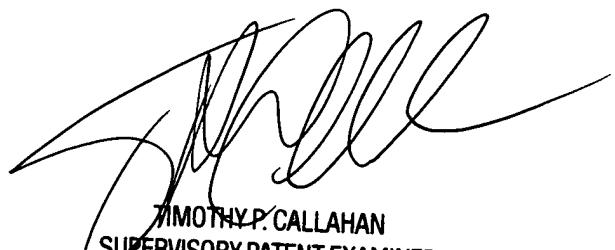
7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
CC
June 09, 2004



TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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